Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a shielding film and a gate signal line formed on an insulating surface;

a planarization insulating film formed ~~on the insulating surface~~ so as to cover the shielding film and the gate signal line; and

a semiconductor layer formed ~~so as to be in contact with~~ over the planarization insulating film,

wherein the shielding film overlaps the semiconductor layer with the planarization insulating film sandwiched therebetween, and

wherein the planarization insulating film is polished [[by CMP]] before the semiconductor layer is formed.

2. (Currently Amended) A device according to claim 1, wherein ~~a thickness~~ thicknesses of the shielding film [[is]] and the gate signal line are 0.1 μm to 0.5 μm.

3. (Currently Amended) A device according to claim 1, wherein the shielding film [[is]] and the gate signal line are tapered around the edge.

4. (Original) A digital camera comprising a semiconductor device according to claim 1.

5. (Original) A video camera comprising a semiconductor device according to claim 1.

6. (Original) A goggle type display device comprising a semiconductor device according to claim 1.

7. (Original) An audio system comprising a semiconductor device according to claim 1.

8. (Original) A notebook personal computer comprising a semiconductor device according to claim 1.

9. (Original) A portable information terminal comprising a semiconductor device according to claim 1.

10. (Original) A DVD player comprising a semiconductor device according to claim 1.

11. (Currently Amended) A semiconductor device comprising:

a shielding film and a gate signal line formed on an insulating surface;

a planarization insulating film formed ~~on the insulating surface~~ so as to cover the shielding film and the gate signal line; and

a thin film transistor including an active layer, the transistor being formed ~~so as to be in contact with~~ over the planarization insulating film,

wherein the active layer has a channel formation region,

wherein the shielding film overlaps the [[entire]] channel formation region with the planarization insulating film sandwiched therebetween, and

wherein the planarization insulating film is polished [[by CMP]] before the active layer is formed.

12. (Currently Amended) A device according to claim 11, wherein ~~a thickness~~ thicknesses of the shielding film [[is]] and the gate signal line are 0.1 μm to 0.5 μm.

13. (Currently Amended) A device according to claim 11, wherein the shielding film [[is]] and the gate signal line are tapered around the edge.

14. (Original) A digital camera comprising a semiconductor device according to claim 11.

15. (Original) A video camera comprising a semiconductor device according to claim 11.

16. (Original) A goggle type display device comprising a semiconductor device according to claim 11.

17. (Original) An audio system comprising a semiconductor device according to claim 11.

18. (Original) A notebook personal computer comprising a semiconductor device according to claim 11.

19. (Original) A portable information terminal comprising a semiconductor device according to claim 11.

20. (Original) A DVD player comprising a semiconductor device according to claim 11.

21. (Currently Amended) A semiconductor device comprising:

a lower layer capacitance wiring and a gate signal line formed on an insulating surface;

a planarization insulating film formed over the lower layer capacitance wiring and the gate signal line;

a capacitance wiring formed ~~so as to be in contact with~~ over the planarization insulating film; and

a pixel electrode electrically connected to the capacitance wiring,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween, and

wherein the planarization insulating film is polished [[by CMP]] before the capacitance wiring is formed.

22. (Currently Amended) A device according to claim 21, wherein ~~the thickness~~ thicknesses of the lower layer capacitance wiring [[is]] and the gate signal line are 0.1 μm to 0.5 μm.

23. (Currently Amended) A device according to claim 21, wherein the lower layer capacitance wiring [[is]] and the gate signal line are tapered around the edge.

24. (Original) A device according to claim 21, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

25. (Original) A digital camera comprising a semiconductor device according to claim 21.

26. (Original) A video camera comprising a semiconductor device according to claim 21.

27. (Original) A goggle type display device comprising a semiconductor device according to claim 21.

28. (Original) An audio system comprising a semiconductor device according to claim 21.

29. (Original) A notebook personal computer comprising a semiconductor device according to claim 21.

30. (Original) A portable information terminal comprising a semiconductor device according to claim 21.

31. (Original) A DVD player comprising a semiconductor device according to claim 21.

32. (Currently Amended) A semiconductor device comprising:

a shielding film, a lower layer capacitance wiring and a lower layer wiring ~~that are~~ formed on an insulating surface;

a planarization insulating film formed ~~on the insulating surface so as to cover~~ over the shielding film, the lower layer capacitance wiring and the lower layer wiring;

a thin film transistor including an active layer, the thin film transistor being formed over the planarization insulating film; and

a capacitance wiring formed over the planarization insulating film,

wherein the active layer has a channel formation region,

wherein the shielding film overlaps the [[entire]] channel formation region with the planarization insulating film sandwiched therebetween,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween,

wherein the thin film transistor has a gate electrode electrically connected to the lower layer wiring, and

wherein the planarization insulating film is polished [[by CMP]] before the active layer is formed.

33. (Original) A device according to claim 32, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring each has a thickness of 0.1 μm to 0.5 μm.

34. (Original) A device according to claim 32, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring are tapered around their edges.

35. (Original) A device according to claim 32, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

36. (Original) A digital camera comprising a semiconductor device according to claim 32.

37. (Original) A video camera comprising a semiconductor device according to claim 32.

38. (Original) A goggle type display device comprising a semiconductor device according to claim 32.

39. (Original) An audio system comprising a semiconductor device according to claim 32.

40. (Original) A notebook personal computer comprising a semiconductor device according to claim 32.

41. (Original) A portable information terminal comprising a semiconductor device according to claim 32.

42. (Original) A DVD player comprising a semiconductor device according to claim 32.

43. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a shielding film ~~that is in contact with~~ and a gate signal line over an insulating surface;

forming an insulating film ~~on the insulating surface~~ so as to cover the shielding film and the gate signal line;

polishing the insulating film [[by CMP]] to form a planarization insulating film; and

forming a semiconductor layer ~~such that it is in contact with~~ over the planarization insulating film,

wherein the shielding film overlaps the semiconductor layer with the planarization insulating film sandwiched therebetween.

44. (Currently Amended) A method according to claim 43, wherein ~~the thickness~~ thicknesses of the shielding film [[is]] and the gate signal line are 0.1 μm to 0.5 μm.

45. (Currently Amended) A method according to claim 43, wherein the shielding film [[is]] and the gate signal line are tapered around the edge.

46. (Original) A method according to claim 43, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

47. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a shielding film ~~that is in contact with~~ and a gate signal line over an insulating surface;

forming an insulating film ~~on the insulating surface~~ so as to cover the shielding film and the gate signal line;

polishing the insulating film [[by CMP]] to form a planarization insulating film; and

forming a thin film transistor including an active layer ~~such that it is in contact with~~ over the planarization insulating film,

wherein the active layer has a channel formation region, and

wherein the shielding film overlaps the [[entire]] channel formation region with the planarization insulating film sandwiched therebetween.

48. (Currently Amended) A method according to claim 47, wherein ~~the thickness~~ thicknesses of the shielding film [[is]] and the gate signal line are 0.1 μm to 0.5 μm.

49. (Currently Amended) A method according to claim 47, wherein the shielding film [[is]] and the gate signal line are tapered around the edge.

50. (Original) A method according to claim 47, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

51. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a lower layer capacitance wiring and a gate signal line over an insulating surface;

forming an insulating film over the lower layer capacitance wiring and the gate signal line;

polishing the insulating film [[by CMP]] to form a planarization insulating film;

forming a capacitance wiring ~~such that it is in contact with~~ over the planarization insulating film; and

forming a pixel electrode electrically connected to the capacitance wiring,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween.

52. (Currently Amended) A method according to claim 51, wherein [[the]] thickness of the lower layer capacitance wiring [[is]] and the gate signal line are 0.1 μm to 0.5 μm.

53. (Currently Amended) A method according to claim 51, wherein the lower layer capacitance wiring [[is]] and the gate signal line are tapered around the edge.

54. (Original) A method according to claim 51, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

55. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a shielding film, a lower layer capacitance wiring and a lower layer wiring ~~that are in contact with~~ over an insulating surface;

forming an insulating film ~~on the insulating surface~~ so as to cover the shielding film, the lower layer capacitance wiring and the lower layer wiring;

polishing the insulating film [[by CMP]] to form a planarization insulating film; and

forming a capacitance wiring and a thin film transistor that includes an active layer over the planarization insulating film,

wherein the active layer has a channel formation region,

wherein the shielding film overlaps the [[entire]] channel formation region with the planarization insulating film sandwiched therebetween,

wherein the lower layer capacitance wiring overlaps the capacitance wiring with the planarization insulating film sandwiched therebetween, and

wherein the thin film transistor has a gate electrode electrically connected to the lower layer wiring.

56. (Original) A method according to claim 55, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring each has a thickness of 0.1 μm to 0.5 μm.

57. (Original) A method according to claim 55, wherein the shielding film, the lower layer capacitance wiring and the lower layer wiring are tapered around their edges.

58. (Original) A method according to claim 55, wherein the thickness of the planarization insulating film is 0.5 μm to 1.5 μm.

59. (New) The method of manufacturing a semiconductor device according to claim 43, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

60. (New) The method of manufacturing a semiconductor device according to claim 47, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

61. (New) The method of manufacturing a semiconductor device according to claim 51, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

62. (New) The method of manufacturing a semiconductor device according to claim 55, wherein the semiconductor device is incorporated into an electronic appliance selected from the group consisting of a video camera, a digital camera, a projector, a head mounted display, a game equipment, a personal computer, a portable telephone, a navigation system, an electronic book, an audio system, a DVD player and a mobile computer.

63. (New) The semiconductor device according to claim 1, wherein the planarization film is polished by CMP.

64. (New) The semiconductor device according to claim 11, wherein the planarization film is polished by CMP.

65. (New) The semiconductor device according to claim 21, wherein the planarization film is polished by CMP.

66. (New) The semiconductor device according to claim 32, wherein the planarization film is polished by CMP.

67. (New) The method of manufacturing a semiconductor device according to claim 43, wherein the insulating film is polished by CMP.

68. (New) The method of manufacturing a semiconductor device according to claim 47, wherein the insulating film is polished by CMP.

69. (New) The method of manufacturing a semiconductor device according to claim 51, wherein the insulating film is polished by CMP.

70. (New) The method of manufacturing a semiconductor device according to claim 55, wherein the insulating film is polished by CMP.

71. (New) The semiconductor device according to claim 1, wherein the insulating surface is a surface of a substrate.

72. (New) The semiconductor device according to claim 11, wherein the insulating surface is a surface of a substrate.

73. (New) The semiconductor device according to claim 21, wherein the insulating surface is a surface of a substrate.

74. (New) The semiconductor device according to claim 32, wherein the insulating surface is a surface of a substrate.

75. (New) The method of manufacturing a semiconductor device according to claim 43, wherein the insulating surface is a surface of a substrate.

76. (New) The method of manufacturing a semiconductor device according to claim 47, wherein the insulating surface is a surface of a substrate.

77. (New) The method of manufacturing a semiconductor device according to claim 51, wherein the insulating surface is a surface of a substrate.

78. (New) The method of manufacturing a semiconductor device according to claim 55, wherein the insulating surface is a surface of a substrate.